

What is Claimed is:

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1 1. An interface between a joystick device and a
2 processor, comprising:
3 a buffer circuit, in a first operation mode of
4 said interface, receiving an analog joystick position
5 measurement signal from said joystick device,
6 outputting a first logic state as a digital signal
7 before said analog joystick measurement signal exceeds
8 said predetermined threshold, and outputting a second
9 logic state as said digital signal after said analog
10 joystick measurement signal exceeds said predetermined
11 threshold; and
12 a pulse generator generating a pulse based on said
13 digital signal in said first operation mode of said
14 interface, a width of said pulse representing a
15 coordinate position of said joystick device.

1 2. The interface of claim 1, wherein said pulse
2 generator enters a disabled state in response to a
3 control signal from said processor, and said pulse
4 generator does not generate said pulse in said disabled
5 state and does not dissipate power in said disabled
6 state.

1 3. The interface of claim 1, wherein said buffer
2 circuit is connected to a charge storage device, and
3 places said charge storage device in a discharged state
4 in a second operation mode of said interface.

1 4. The interface of claim 3, wherein
2 said buffer circuit permits said charge storage
3 device to begin charging in said first operation mode
4 of said interface.

1 5. The interface of claim 3, wherein said pulse
2 generator enters a disabled state in response to a
3 control signal from said processor in said second
4 operation mode of said interface, and said pulse
5 generator does not generate said pulse in said disabled
6 state.

1 6. The interface of claim 1, wherein said pulse
2 generator is a latch.

1 7. The interface of claim 6, wherein said latch
2 is cleared at a beginning of said first operation mode
3 of said interface by a control signal from said
4 processor, and said latch stores a logic "1" when said
5 digital signal is said second logic state.

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1 8. The interface of claim 1, further comprising:
2 a Resistor-Capacitor (RC) network, connected to
3 said joystick device, generating said analog joystick
4 position measurement signal, said RC network capacitor
5 being preselected in accordance with the formula:

$$C_{new} = \frac{11nF}{\ln\left(\frac{5V}{5V - V_{new}}\right)} \text{ for } V_{new} < 5.0 \text{ Volts,}$$

6
7 where C_{new} represents the capacitance of the RC network
8 capacitor, and V_{new} represents said predetermined
9 threshold.

1 9. A processor based system, comprising:
2 a processor:

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3 a joystick device;
4 an interface interfacing said joystick device with
5 said processor, said interface including,
6 a buffer circuit, in a first operation mode
7 of said interface, receiving an analog joystick
8 position measurement signal from said joystick device,
9 outputting a first logic state as a digital signal
10 before said analog joystick measurement signal exceeds
11 said predetermined threshold, and outputting a second
12 logic state as said digital signal after said analog
13 joystick measurement signal exceeds said predetermined
14 threshold, and
15 a pulse generator generating a pulse based on
16 said digital signal in said first operation mode of
17 said interface, a width of said pulse representing a
18 coordinate position of said joystick device, and
19 outputting said pulse to said processor.

1 10. The processor based system of claim 9, wherein
2 said pulse generator enters a disabled state in
3 response to a control signal from said processor, and
4 said pulse generator does not generate said pulse in
5 said disabled state and does not dissipate power in
6 said disabled state.

1 11. The processor based system of claim 9,
2 wherein said buffer circuit is connected to a charge
3 storage device, places said charge storage device in a
4 discharged state in a second operation mode of said
5 interface, and permits said charge storage device to
6 begin charging in said first operation mode of said
7 interface.

1 12. The processor based system of claim 9,
2 wherein said pulse generator is a latch, said latch is
3 cleared at a beginning of said first operation mode of
4 said interface by a control signal from said processor,

4 said interface by a control signal from said processor,
5 and said latch stores a logic "1" when said digital
6 signal is said second logic state.

1 13. The interface of claim 9, further comprising:
2 a Resistor-Capacitor (RCA) network, connected to
3 said joystick device, generating said analog joystick
4 position measurement signal, said RC network capacitor
5 being preselected in accordance with the formula:

$$C_{new} = \frac{11nF}{\ln\left(\frac{5V}{5V - V_{tnew}}\right)} \text{ for } V_{tnew} < 5.0 \text{ Volts,}$$

6
7 where Cnew represents the capacitance of the RC network
8 capacitor, and Vtnew represents said predetermined
9 threshold.

1 14. A method of interfacing a joystick device
2 with a processor, comprising:

3 (a) receiving an analog joystick measurement
4 signal from said joystick device;

5 (b) generating a digital signal, the logic level
6 of said first digital signal being set based on whether
7 said analog joystick measurement signal exceeds a
8 predetermined threshold level,

9 (c) outputting said digital signal to a pulse
10 generator;

11 (d) generating a pulse based on the logic level
12 of said first digital signal, a width of said pulse
13 representing a coordinate position of said joystick
14 device; and

15 (e) outputting said pulse to said processor.

1 15. The method according to claim 14, wherein
2 said steps (a) - (e) are performed in a first mode of
3 operation.

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1 16. The method of claim 15, wherein
2 said step (a) receives said analog joystick
3 measurement signal via a charge storage device; and
4 further including,
5 (f) placing said charge storage device in a
6 discharged state in a second mode of operation.

1 17. The method of claim 16, further comprising:
2 (g) permitting said charge storage device to begin
3 charging in said first mode of operation.

1 18. The method of claim 16, further comprising:
2 (g) prohibiting said steps (d) and (e) in response
3 to a control signal from said processor in said second
4 mode of operation.

1 19. The method of claim 14, further comprising:
2 (f) prohibiting said steps (d) and (e) in response
3 to a control signal from said processor.

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1 20. The method of claim 14, wherein said analog
2 joystick measurement signal is generated by a Resistor-
3 Capacitor (RC) network capacitor connected to said
4 joystick device, and said method further comprises:
5 (f) preselecting the RC network capacitor in
6 accordance with the formula:

$$C_{new} = \frac{1 \text{ nF}}{\ln\left(\frac{5V}{5V - V_{tnew}}\right)} \text{ for } V_{tnew} < 5.0 \text{ Volts,}$$

7
8 where C_{new} represents the capacitance of the RC network
9 capacitor, and V_{tnew} represents said predetermined
10 threshold level.

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